MICHAEL D. POWELL

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EDUCATION

Ph.D., Electrical and Computer Engineering, 1999-2005
Purdue University, School of Electrical and Computer Engineering
Dissertation: "Microarchitectural Techniques for Power-Related Issues in Scaled Technologies"
Advisor: T. N. Vijaykumar
GPA 3.5/4.0

BS Electrical Engineering, 1996-1999
Purdue University, Electrical and Computer Engineering
Degree awarded with highest distinction
GPA 4.0/4.0
Minor in political science

WORK EXPERIENCE

Senior Design Engineer, Fault Aware Computing Technology (FACT) Group and Technology for Reliability and Usage (TRU) Group, Intel Massachusetts, September, 2005 – present

- Product pathfinding and advanced development for managing process variation and hard faults:
  - Proposed architectural enhancements based on analysis of thousands of CPU die over 3 product generations to improve performance by approximately 10% by optimizing for process variation.
  - Supervised a graduate intern project studying using intra-core microarchitectural redundancy to tolerate faults. Integrated into Intel's yield model to estimate yield improvement and published an internal paper. Proposed follow-on studies on cross-core architectural redundancy, developed model, and produced results indicating potential performance/yield recovery. Published an external paper proposing cross-core redundancy as a high-performance salvaging technique for defective CPU cores.
  - Developed architectural hard-fault model and utilization model and supervised graduate intern on proof-of-concept implementations.
  - Along with external consultant, evaluated hard failure modes and sensors for detecting errors.

- Extensive architectural power modeling experience for both research and product-development:
  - Developed Intel's first integrated full-system power management and performance model enabling power-management feature evaluation of future products on full-system workloads.
  - Developed methodology for estimating fine-grained structure power in hardware and supervised a graduate intern in developing this model. Published the methodology and results externally and applied this methodology to develop power models for several CPU products.
  - Developed parameterized CPU core power model for a product. Responsible for core power equations and power-model infrastructure in the product performance simulator.

- Member of architecture team for a future flagship IA (x86) product
  - Explored power-performance analysis for fixed-function and programmable accelerators for future server product.
  - Developed analytical models for high fault rate CPU and architecture behavior.
  - Developed proposals for reducing guardbands to improve performance.

- Managed an ongoing faculty consulting agreement/collaboration from 2006-2011, providing research direction for development of invention disclosures and whitepapers on circuit reliability topics.
- Supervised 4 full-time doctoral-student intern projects and 2 part-time doctoral-student intern projects.
- Extensive experience with C/C++ performance, power, power-management, full-system (Simics), and instruction-architecture models. Performed IA (x86) 64-bit microcode corner-case debug to match performance model behavior to golden architecture specification.

Intern, Tellabs VLSI Design Department, Summer 1999 and Summer 1998
Undergrad Research Assistant, Purdue Center for Collaborative Manufacturing (NSF ERC), 1997-1998
Undergrad Teaching Assistant, Purdue Freshman Engineering, Honors Computer Tools/Programming; 1997-1999

HONORS AND AWARDS
Division Recognition Award, Intel, 2007
National Science Foundation Graduate Research Fellowship, 1999-2004
Intel Ph.D. Fellowship, 2002-2003
National Merit Scholarship, 1996-1999; Robert C. Byrd Scholarship, 1996-1999

PROFESSIONAL SOCIETY MEMBERSHIP
IEEE Senior Member (student member or member since 1996)
Eta Kappa Nu (Beta Chapter President, Spring 1999)
Tau Beta Pi

SELECTED EXTERNAL PUBLICATIONS

K. K. Rangan, M. D. Powell, G.-Y. Wei, and D. Brooks, "Achieving Uniform Performance and Maximizing Throughput in the Presence of Heterogeneity," 17th International Symposium on High Performance Computer Architecture (HPCA 17), February 2011.

M. D. Powell, A. Biswas, S. Gupta, and S. S. Mukherjee, "Architectural Core Salvaging in a Multi-Core Processor for Hard-Error Tolerance," 36th International Symposium on Computer Architecture (ISCA 36), June 2009. (accept 43 out of 210 submissions)

M. D. Powell, A. Biswas, J. S. Emer, S. S. Mukherjee, B. R. Sheikh, and S. Yardi, "CAMP: A Technique to Estimate Per-Structure Power at Run-time using a Few Simple Parameters," 15th International Symposium on High Performance Computer Architecture (HPCA 15), February 2009. (accept 35 out of 184 submissions)

M. D. Powell and T. N. Vijaykumar, "Resource Area Dilation to Reduce Power Density in Throughput Servers," International Symposium on Low Power Electronics and Design (ISLPED), August 2007. (accept 57 out of 192 submissions, not counting posters)

M. D. Powell, Ethan Schuchman, and T. N. Vijaykumar, "Balancing Resource Utilization to Mitigate Power Density in Processor Pipelines," 38th International Symposium on Microarchitecture (MICRO 38), December 2005. (accept 29 out of 147 submissions, not counting posters)

Z. Chishti, M. D. Powell, and T. N. Vijaykumar, "Optimizing Replication, Communication, and Capacity Allocation in CMPs," 32nd International Symposium on Computer Architecture (ISCA 32), June 2005. (accept 45 out of 194 submissions)

M. D. Powell, M. A. Gomaa, and T. N. Vijaykumar, "Heat and Run: Leveraging SMT and CMP to Manage Power Density Through the Operating System," 11th International Conference on Architectural Support for

Programming Languages and Operating Systems (ASPLOS 11), pages 260-270, October 2004. (accept 24 out of 169 submissions)

M. D. Powell and T. N. Vijaykumar, "Exploiting Resonant Behavior to Reduce Inductive Noise," 31st International Symposium on Computer Architecture (ISCA 31), pages 288-299, June 2004. (accept 31 out of 218 submissions)

Z. Chishti, M. D. Powell, and T. N. Vijaykumar, "Distance Associativity for High-Performance Energy-Efficient Non-Uniform Cache Architectures," International Symposium on Microarchitecture (MICRO 36), pages 55-66, December 2003. (accept 34 out of 135 submissions)

M. D. Powell and T. N. Vijaykumar, "Pipeline Muffling and A Priori Current Ramping: Architectural Techniques to Reduce High-Frequency Inductive Noise," International Symposium on Low Power Electronics and Design (ISLPED), pages 223-228, August 2003. (accept 54 out of 221 submissions, not counting posters)

M. D. Powell and T. N. Vijaykumar, "Pipeline Damping: A Microarchitectural Technique to Reduce Inductive Noise in Supply Voltage," International Symposium on Computer Architecture (ISCA 30), pages 72-83, June 2003. (accept 36 out of 184 submissions)

I. Park, M. D. Powell, and T. N. Vijaykumar, "Reducing Register Ports for Higher Speed and Lower Energy," International Symposium on Microarchitecture (MICRO 35), pages 171-181, November 2002. (accept 36 out of 150 submissions)

S. H. Yang, M. D. Powell, B. Falsafi, and T. N. Vijaykumar, "Exploiting Choice in Resizable Cache Design to Optimize Deep-Submicron Processor Energy-Delay," International Symposium on High Performance Computer Architecture (HPCA 8), pages 147-158, February 2002. (accept 26 out of 130 submissions)

M. D. Powell, A. Agarwal, T. N. Vijaykumar, B. Falsafi, and K. Roy, "Reducing Set-Associative Cache Energy via Selective Direct-Mapping and Way Prediction," International Symposium on Microarchitecture (MICRO 34), pages 54-65, December 2001. (accept 29 out of 144 submissions)

S. H. Yang, M. D. Powell, B. Falsafi, K. Roy, and T. N. Vijaykumar, "An Integrated Circuit/Architecture Approach to Reducing Leakage in Deep-Submicron High-Performance I-Caches," International Symposium on High Performance Computer Architecture (HPCA 7), pages 147-158, January 2001. (accept 26 out of 110 submissions)

M. D. Powell, S.H. Yang, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Reducing Leakage in a High-Performance Deep-Submicron Instruction Cache," IEEE Transactions on VLSI, Special Issue on Low Power Electronics and Design, February 2001.

M. D. Powell, S. H. Yang, B. Falsafi, K. Roy, and T. N. Vijaykumar, "Gated-Vdd: A Circuit Technique to Reduce Leakage in Deep-Submicron Cache Memories," International Symposium on Low Power Electronics and Design (ISLPED), pages 90-95, July 2000. (accept 39 out of 162 submissions, not counting posters)

PATENTS

Steven Raasch, Michael D. Powell, Arijit Biswas, and Shubhendu S. Mukherjee, “Using General Purpose Hardware to Replace Faulty Core Components,” filed by Intel, 2010.

PROFESSIONAL ACTIVITIES AND SERVICE

HPCA Industrial Session: Program chair for 2014, program committee member for 2013
HPCA 2013: Web chair

Program Committee Member: Computing Frontiers, 2007
External reviewer for architecture conferences and journals
Purdue ECE Graduate Committee: student member (2004-2005)
Purdue ECE Building Planning Staff Subcommittee: student member (2004)
Purdue ECE Head Search Committee: student member (2001-2002)